



Sheet 1 of 1

Form PTO 1449 (modified)				Docket No <u>YOR920020001US1</u>		Serial No <u>10/085,606</u>	
LIST OF PRIOR ART CITED BY APPLICANT				Applicant <u>Michael Gschwind et. al.</u>			
				Filing Date <u>02/26/2002</u>		Group 2102	
U. S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
<u>TM</u>	AA	5,864,341	01/26/1999	Hicks	395	390	12/06/1996
	AB						
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Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
OTHER PRIOR ART ( Including Author, Title, Date, Pertinent Pages, Etc.)							
<u>TM</u>				C. Zilles and G. Sohi "Understanding the Backward Slices of Performance Degrading Instructions", Proc. of the International Symposium on Computer Architecture, 2000. pp: 172 -181			
<u>TM</u>				K. Ebcioglu, et al "Optimizations and Oracle Parallelism with Dynamic Translation", Proc. of the 32nd International Symposium on Microarchitecture, 1999. pp.: 284-295			
<u>TM</u>				S. Abraham, et al, "Predictability of Load/Store Instruction Latencies", Proc. of the 26th International Symposium on Microarchitecture, 1993. pp.:139-152			
<u>TM</u>				M. Annavaram, et al "Data Prefetching by Dependence Graph Precomputation", Proc. of the International Symposium on Computer Architecture, 2001. pp.: 52-61			
<u>TM</u>				S. Srinivasan et al, "Locality vs. Criticality", Proc. of the International Symposium on Computer Architecture, 2001., pp.: 132-143			
Examiner	<u>Donna Heenske</u>			Date Considered	<u>July 26, 2004</u>		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MREP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant							

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